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STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
PLANTE, JONATHAN R	
ART UNIT	**PAPER NUMBER**
2182	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/812,103	SMITH ET AL.	
	Examiner	Art Unit	
	Jonathan R. Plante	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 May 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED NON-FINAL ACTION

1. This Office Action is in response to the applicant's communication filed 21 May 2007 in response to PTO Office Action mailed 20 November 2006. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

Drawing Amendments

2. Acknowledgement of receiving replacement drawings, which were received by the Office on 21 May 2007. These drawings are Figure 1 and 2.

The following objections to the drawings have **NOT** been withdrawn due to amendment filed on 21 May 2007.

3 (a): Number/index the figures appropriately,

Examiner requested that reference characters be added to the written specification and drawings in order to indicate components/elements that Applicant has disclosed and discussed as elements of the invention in order to facilitate the understanding and correspondence of the written description and the drawings.

3 (b): Replace "**FIG. 1 (State of the Art)**" with "FIG. 1 (Prior Art)",

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

In response to Applicant's remarks (Page 8, "Objections to the Drawings") filed on 21 May 2007 in respect to the term "state of the art" Examiner is not persuaded. The term "state of the art" is a relative term and does not clearly and precisely indicated the knowledge associated with Figure 1. Additionally the Examiner notes that if Figure 1 is the "state of the art" then inherently it is "prior art" since it is knowledge that existed prior to the date of Applicants invention.

Objection 3 (c) to the drawings has been withdrawn due to amendment filed on 21 May 2007.

New Drawings Objections

3. The drawings are objected to because:

    a. (Figures 1, 2): The multiplexer (mux) depicted in Figures 1 and 2 depicts a signal connecting to mux input 0 and the clock input of the latch proceeding the mux. This results in an input (mux 0) being feed by an input (clock) of the latch. As a result there is an input-to-input connection, and not an output-to-input connection. Applicant is requested to correct the drawings in order to elevate this discrepancy.

    b. (Figures 1, 2): The labeling of inputs "Latch" and "Data" are undefined and cause confusion and ambiguity as to what signals they represent. Since Applicant has failed to disclose/describe "Latch" and "Data" in the specification it will be the Examiners interpretation that the terms "Latch" and "Data" simply represent generic input data.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief

description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification Amendments

4. Acknowledgement of receiving amendments to the specification, which were received by the Office on 21 May 2007. The specification has been updated according to reflect amendments.

The following objections to the specification have **NOT** been withdrawn due to amendment filed on 21 May 2007.

5 (f): Please replace "**NCVerilog**" (Page 2, Line 14) with "NCVerilog ®".

The use of the trademark "NCVerilog" has been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

5 (iii): Please insert "**(ASIC)**" (Page 9, Line 9) after "integrated circuits".

The Examiner requested the insertion of "ASIC" to be consistent with terminology used in the art in that "ASIC" is a general use acronym in the art for an "application specific integrated circuit". Additionally the acronym "ASIC" is a common search term used in the art and would facilitate future examiners searches and benefits the Applicant in respect to searches of prior art where Applicants disclosure would be applicable.

New Specification Objections

5. The use of the trademarks "Verilog" (Page 2, Line 13) and "Cadence" (Page 2, Line 14) have been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

   a. (Page 2, Line 13): Please replace "**Verilog**" with "Verilog ®" to resolve trademark issues.

b. (Page 2, Line 14): Please replace "**Cadence**" with "Cadence ®" to resolve trademark issues.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

Claim Amendments

6. Acknowledgment of receiving amendments to the claims, which were received by the Office on 21 May 2007. Claims 8, 9, and 10 are amended.

The objections to the claims have been withdrawn due to amendment filed on 21 May 2007.

Claim Rejections - 35 USC § 101

7. The 35 USC § 101 rejections to the claims have been withdrawn as a result of new policies associated with disclosing a "tangible result" within the written description as being sufficient to fulfill the "tangible result" requirements of 35 USC § 101 in respect to the claimed subject matter.

Claim Rejections - 35 USC § 112

8. The 35 USC § 112 rejections to Claims 8, 12, and 13 have been withdrawn due to amendment filed on 21 May 2007.

   The 35 USC § 112 rejection to Claim 9 has **NOT** been withdrawn due to amendment filed on 21 May 2007.

   Applicant has not addressed the rejection to Claim 9 (Office Action 20 November 2006, Page 11) in amendment filed on 21 May 2007.

9. The following is a quotation of the first paragraph of 35 U.S.C. 112:

   > The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. Claim 9 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

    As per claim 9, the applicant claims, "the simulation is carried out on a cycle level of a description" (Claim 9, Line 1), and according to the specification "In cycle level simulations logic functions effectively happen

in zero time, so generally all signals appear to change at the same time." (Page 2, Line 19). Claim 9 is rejected for the failure of the applicant to disclose to one skilled in the art how a "cycle level" description/simulation accounts for the "jitter elements" (Claim 8, Line 3) defined as "Jitter elements according to the invention comprise delay elements and x generator elements" (Page 7, Line 5) in the simulation. The application and review of the prior art define a "cycle level" simulation, as a simulation that does not account for timing, slew, and/or logic delay meaning that a "cycle level" simulation only evaluates the functional status of the circuit. As a result the applicant has claimed the application of a "cycle level" simulation with the application of timing delay elements, but has failed to disclose how the "cycle level" simulation has been modified to account for timing. The usage of a non-timing simulation technique ~~it~~ is at opposition with the application of added elements for the purpose of increasing the time delays.

For purpose of this office action the examiner will interpret the "cycle level" simulation to be defined as "Cycle based simulations allow the designer to examine the results at the end of a cycle. A cycle based simulator does not have to determine the propagation delay of the logic elements in the design." Vaidyanathan et al. (US 5,809,283) (Column 2, Line 4), and for the evaluation of claims relating to the application of timing delay a "event-driven" simulation will be applied and defined as "Event-driven simulators propagate signals from the output of one system element to the inputs of the next system element and allow the designer to examine the results of the propagation throughout a clock cycle. Additionally, the event-driven simulators simulate the propagation delay of the logic elements in the design." Vaidyanathan et al. (US 5,809,283) (Column 1, Line 64). It is the opinion of the examiner that these definitions for "cycle" and "event-driven" simulations are uniform definitions for individuals skilled in the art, based on prior art and knowledge of one skilled in the art.

(Office Action 20 November 2006, Page 11)

Claim Rejections - 35 USC § 102

11. The 35 USC § 102 rejections to Claims 8-13 have been withdrawn due to amendment filed on 21 May 2007. Applicant's arguments, see Pages 11-15,

filed 21 May 2007, with respect to Office Action mailed 20 November 2006 have been fully considered and are persuasive.

New Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

13. Claims 8, 9, 11, 12, and 13 are rejected under 35 U.S.C. 102(a) as being anticipated by Benis (US 2003/0125916 A1 July 3, 2003).

(Claim 8): Benis discloses, "Simulation system for simulation of an electronic circuit, the circuit being representable by a network of logical elements, **[*simulation* (ABSTRACT)]** the circuit comprising a first and second asynchronous clock domain, **[*asynchronous clock domain* (Paragraph 0002)]** wherein jitter elements **[*random number generator* (Figure 4A, 470)]** are additionally insertable at predetermined portions of circuit boundaries between the first and second asynchronous clock domain, **[*random number generator and associated registers are inserted to model metastable effects and are inherently inserted between asynchronous clock domains* (Paragraph 0035)]** the jitter elements being representable as logical elements, **[*multiplexers***

and registers **(Paragraph 0036)]** the values of which are randomly set." **[*random number generator*** **(Figure 4A, 470)].**

(Claim 9): Benis discloses, "wherein the simulation is carried out on a cycle level of a description of the electronic circuit." as **["hardware description languages such as Verilog" (Paragraph 0057)].**

(Claim 11): Benis discloses, "wherein the jitter elements comprise x generator elements for introducing predetermined signal values which are randomly generated." as **[RANDOM NUMBER GENERATOR" (Figure 4A, 470)].**

(Claim 12): Benis discloses, "wherein the jitter elements are interactively inserted by a user." as **[*user is capable of entering information and performing command selections via a user interface and input device*** **(Paragraph 0027)].**

(Claim 13): Benis discloses, "wherein the jitter elements are automatically inserted using predetermined modules." as **[*multiplexers 460, 480, and 482 in addition to the random number generator are simulated by the simulation*** **(Paragraph 0036)** ***and it is inherent that the simulation program inserts these simulation for each asynchronous interface to test for metastability*****].**

14. Claims 8, 9, 10, 12, and 13 are rejected under 35 U.S.C. 102(a) as being anticipated by Sharma et al. (US 6,598,191 B1 July 22, 2003).

(Claim 8): Sharma et al. discloses, "Simulation system for simulation of an electronic circuit, the circuit being representable by a network of logical elements, **[*hardware emulator* (Column 2, Line 15)]** the circuit comprising a first and second asynchronous clock domain, **[*asynchronous clock domain* (Column 1, Line 18)]** wherein jitter elements **[delay register (Column 2, Line 51)]** are additionally insertable at predetermined portions of circuit boundaries between the first and second asynchronous clock domain, **[*the delay register, multiplexer, and random signal selector are positions between the two clock domains* (Column 2-3, Lines 51-5) (Figure 4, Index 108, 102, 114)]** the jitter elements being representable as logical elements, **["EXTENDED FLIP-FLOP LEVEL B", "multiplexer", and "PSEUDO-RANDOM GENERATOR" (Figure 4, Index 108, 114, 102)]** the values of which are randomly set." **["PSEUDO-RANDOM GENERATOR" (Figure 4, 102)].**

(Claim 9): Sharma et al. discloses, "wherein the simulation is carried out on a cycle level of a description of the electronic circuit." As **[*hardware emulator written in C, C++, PASCAL, Verilog, and/or VHDL* (Column 2, Line 15-21)].**

(Claim 10): Sharma et al. discloses, "wherein the jitter elements comprise delay elements for introducing predetermined timing delays which is randomly exercised." as **[*the delay register and multiplexer controlled by the random signal selector are used to randomly exercise the timing delay* (Column 2-3, Lines 51-5)].**

(Claim 12): Sharma et al. discloses, "wherein the jitter elements are interactively inserted by a user." as **[*can be inherently declared in the hardware description using Verilog or similar hardware model software.* (Column 2, Line 15-21)].**

(Claim 13): Sharma et al. discloses, "wherein the jitter elements are automatically inserted using predetermined modules." as **[*the module consisting of the delay register, multiplexer, and random generator can be inserted within any clock domain by the simulation for verifying the asynchronous boundary behavior as part of the simulation and verification* (Column 4, Line 44-48)].**

Conclusion

15. In addition to reference used under 35 U.S.C. 102, additional prior art references that disclose relevant subject matter on the merits can be found in:

    a. Leslie (US 4,575,644 March 11, 1986)

b. Walp (US 5,826,061 October 20, 1998)

c. Nelson (US 4,797,838 January 10, 1989)

d. Ho et al. (US 2005/0131665 A1 June 16, 2005)

e. Schaumont et al. (US 7,006,960 B2 February 28, 2006)

16. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jonathan R. Plante whose telephone number is (571) 272-9780. The examiner can normally be reached on Monday -- Thursday 10:00 AM to 4:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

18. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

June 14, 2007
JRP

Jonathan R. Plante
ART UNIT 2182

6/19/07